

## Course Description

Covers the microarchitecture level of machine design and advanced architecture features for performance enhancement. Topics include computer performance measures, microarchitecture instructions, CPU design (data path, pipelines, control unit, instruction level parallelism), memory hierarchy, cache memory, virtual memory, parallel processing and multicore architectures.

## Course Objectives

The objectives of this course are to teach students:

- Assembly programming
- CPU implementation, i.e. control signals in single and multi-cycle machines
- Pipeline architectures and hazard handling
- Memory hierarchy organization
- Cache and virtual memory organization
- Microprogramming
- Parallel architectures

## Student Learning Outcomes

Upon successful completion of the course, students should be able to:

- Write assembly programs
- Explain the hardware implementation of micro architecture instructions
- Trace the flow of data and control signals through a data path
- Explain the principles of cache and virtual memories
- Explain the principles of parallel processing and multicore architectures

## Course Schedule (TENTATIVE)

Weeks	Topic
1 & 2	<ul style="list-style-type: none"><li>• Syllabus</li><li>• Review of Machine Organization (371) Concepts</li><li>• Introduction to Computer Architecture</li><li>• Performance</li><li>• Heterogeneous Computing</li></ul>

	<ul style="list-style-type: none"> <li>• <a href="https://tues.cs.txstate.edu/modules/a1.php">https://tues.cs.txstate.edu/modules/a1.php</a></li> </ul>
3	<ul style="list-style-type: none"> <li>• MIPS</li> <li>• Quiz 1</li> </ul>
4	<ul style="list-style-type: none"> <li>• ARM</li> <li>• <a href="https://github.com/TeachingUndergradsCHC/modules/tree/master/Architecture/arm%20introduction">https://github.com/TeachingUndergradsCHC/modules/tree/master/Architecture/arm introduction</a></li> </ul>
5	<ul style="list-style-type: none"> <li>• The Processor <ul style="list-style-type: none"> <li>○ Data path</li> <li>○ Pipelining</li> <li>○ Data Hazards</li> <li>○ Control Hazards</li> <li>○ Exceptions</li> <li>○ Parallelism via Instructions</li> </ul> </li> <li>• Quiz 2</li> </ul>
6 & 7	<ul style="list-style-type: none"> <li>• The Processor (Cont.)</li> </ul>
8	<ul style="list-style-type: none"> <li>• Heterogeneous Computing</li> <li>• (Incorporate a research paper or presentation here) <ul style="list-style-type: none"> <li>• <a href="https://tues.cs.txstate.edu/modules/c1.php">https://tues.cs.txstate.edu/modules/c1.php</a></li> </ul> </li> <li>• Quiz 3</li> </ul>
9 & 10	<ul style="list-style-type: none"> <li>• Memory Hierarchy <ul style="list-style-type: none"> <li>○ Types of memory</li> <li>○ Cache Basics</li> <li>○ Virtual Memory</li> </ul> </li> <li>• Quiz 4</li> </ul>

Long term Plan:

- Machine Organization with Raspberry PI, concurrently learn C while learning the concepts
- Computer Architecture with ARM and MIPS (incorporating some parallel hands on work)
- Operating Systems course continues to incorporate parallel programming